REMARKS/ARGUMENTS

In the Office action dated February 2, 2004, the Examiner rejected claims 1-20 and 22, all of the claims pending in the Application. Claims 1, 6, 11, 15 and 17 stand rejected under 35 U.S. C. § 102(b) as being anticipated by U. S. Patent No. 4,703,551 to Szluk *et al.* Claims 2-4, 7-9, 12-14, and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '551 in view of U. S. Patent No. 6,069,044 to Wu. Claims 5, 10, 16 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '551 in view of U. S. Patent No. 5,757,045 to Tsai *et al.*

In the Specification, there are no changes.

In the Claims, claims 1 and 11, all of the independent claims, are currently amended. Claims 6-10 and 17-22 are cancelled.

The Invention

The invention is a method of forming a MOS or CMOS device on a silicon substrate, and implanting MDD or conventional dosage ions in source and drain regions, while simultaneously, and without the need for a separate mask, implanting LDD source and drain regions underlying a gate sidewall. The substrate is prepared, and includes a conductive region of a first type, such as an n-type or p-type conductive region, which has a first device active area therein. Two such regions are prepared, of opposite conductive types, for a CMOS device. A gate electrode is formed on the active area(s), and a gate sidewall is formed about the gate. Ions of an opposite conductivity type to that of the conductive region of the first type are implanted into the conductive region of the first type to form a source region and a drain region on opposite sides of the gate electrode, and to form flanking LDD region adjacent the source and drain and underlying the gate sidewall. An important feature of the invention is the fabrication of a device using only a

single implantation step and a single mask to form the source, drain and associate LDD regions, and the deposition of a silicide layer by selective CVD, which does not require further masking, and which does not, by virtue of the deposition of silicide, as opposed to deposition of a metal and formation of a silicide, or deposition of a silicide layer on as silicon substrate, does not reduce the thickness of the silicon substrate or component. The reduction in implantation and masking steps saves time and reduces the overall cost of the fabrication process. In fact, the method of the invention saves two mask levels during fabrication of a CMOS device, and saves two-ion implantation steps during CMOS fabrication. The silicide layer is formed with only a single, selective CVD process.

The Applied Art

U. S. Patent No. 4,703,551 to Szluk *et al.* describes a method of implantation which requires at least two, and likely three, separate implantation steps. Not only are these multiple implantation steps described in the Specification, the claims of '551 require multiple implantation steps. Elimination of any of the doping steps will render any devices formed by the method of the invention inoperative. One implantation step is described as lightly doping, col. 9, lines 30-50, while another implantation step is described as heavy doping, col. 5, line 66 - col. 6, lines 14. While the Examiner is correct that the source and drain regions are formed in a single implantation step, a second implantation step is required to form LDD source region 31N and LDD drain region 32N. Col. 8, lines 25-29. If the light doping step is conducted with too great an ion dose, the ions will leak into the channel, rendering the device inoperative. Thus, multi-step masking and implantation steps are required by the '551 reference to form the heavily doped source/drain regions and the LDD source/drain regions. A tungsten layer is formed, and is stated to be

equivalent to a refractory metal silicide layer. Col. 9, lines 61- col. 10, line 7. However, yet another masking step is required for this process, and regardless of whether the deposition is metal and a silicide conversion, or a silicide deposition, both take place on a silicon substrate, and will, during subsequent annealing, will reduce the thickness of the silicon substrate.

U. S. Patent No. 5,757,045 to Tsai *et al.* describes a standard silicide process, and also describes, and requires, multiple masking and implantation steps for active area formation in the CMOS. Col. 3, line 65 to col. 5, line 22.

U. S. Patent No. 6,069,044 to Wu describes a multi-step, low energy implantation process.

The Claims

All of the independent claims require that the implant of the second type ions be accomplished using a single mask and in a single implant step to form LDD source/drain regions adjacent regular or MDD implanted source/drain regions. The Examiner's argument that the claims are not so limited (Office action, page 6) because of the standard claim construction use of "comprising" is not correct: while other steps, or elements, could be, and are most certainly used, to construct a usable, marketable device, the language of the claims is quite clear and only subject to a single legal interpretation: that any and all implantation of second type ions must be accomplished using a single mask and in a single step. If the Examiner continues to disagree with Applicants' position, the Examiner is invited to suggest language which will meet this limitation.

The Examiner states that '551 "apparently teaches a solo implantation step to form source/drain regions 28N." However, a close reading of '551 reveals that three separate masking and implantation steps are required to form the three requisite active areas 28N, 32N and 34N:

these structures are formed using the steps as described in col. 6, line 38, through col. 8, line 38. '551 doesn't form any active area in a single mask, single implant step. Likewise, '045 does not teach or suggest single mask, single step ion implantation as taught and claimed by Applicants. All of the independent claims stand rejected under 35 U.S. C. § 102, yet the Examiner goes beyond the teachings of the applied references to provide a reasons for rejecting the claims under 35 U.S. C. § 102, which is akin to a 35 U.S.C. § 103(a) rejection, however, as the rejection is under 35 U.S. C. § 102, Applicants must respond to the rejection as stated. Applicants teach the formation of a MOS or CMOS device using a single mask and single step ion implantation for second type ions - they do not go beyond the scope of the recited language. The Examiner has broadened Applicants' claims, and then rejected them based on art which uses multiple masks and implantation steps. Such is not a proper 35 U.S. C. § 102 rejection.

Claim 1 recites steps of the method of the invention to form a MOS device, and has been amended to recite that the source and drain regions include a LDD region underlying the insulating sidewall of the gate electrode. Although no provided with a separate reference number in the drawings, referring to Figs. 3 and 4, source 30 and drain 32 may be seen to underlie gate sidewall 22. Likewise, drain 38 and source 40 underlie sidewall 24. During the implantation step described in the Specification, page 6, line 18 through page 7, line 19, it will be well understood and appreciated by those of ordinary skill in the art that the ion resulting ion concentration for the portions of the source and drain regions underlying the gate sidewall will be significantly less than in the portions of the exposed source and drain regions. The Specification, page 1, line 23, through page 2, line 9 recites the purpose of the sequence of the steps of the method of the invention as providing for both regular or MDD source/drain regions and for LDD source/drain regions in a

single masking and implant step. The applied art does not teach nor suggest the method of the invention, and claim 1 is allowable over the prior art of record.

Claims 2-5 are allowable with their allowable parent claim.

Claim 11 has been amended to recites steps similar to those of claim 1 for fabrication of a CMOS device, and is allowable for the reasons set forth in connection therewith.

Claims 12-16 are allowable with their allowable parent claim.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections stated in the Office action, and pass the application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Provisional Request for Extension of time in Which to Respond

Should this response be deemed to be untimely, Applicants hereby request an extension of time under 37 C.F.R. § 1.136. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any over-payment to Account No. 19-1457.

Respectfully submitted,

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